REMARKS

Claims 1-41 are pending in this application. Claims 11-18 and 30-39 have been withdrawn from consideration. Claims 1-10, 19-29, and 40-41 have been examined and rejected.

Applicant has amended claims 1, 3, 19, 27, and 29 as indicated above for the reasons described herein.

Restriction Requirement

The Office considered Applicant's arguments about why the restriction requirement is improper and made "election of [the elected] device claims final." Importantly, the Office provided no reason why Applicant's arguments were not persuasive.

By not providing any reasoning, the Office has improperly made the restriction requirement final. M.P.E.P. § 821.01 requires that where the Office makes a restriction requirement final, it must "reply to the reasons or arguments advanced by [A]pplicant in the traverse." The Office has not made such a reply. Therefore, the Office has not established a proper restriction requirement and it should be withdrawn.

Drawings

The Office has objected to the drawings for the reasons set forth on page 2 of the Office Action. In response to the argument that the n-type substrate recited in claim 3 is not shown, Applicant has amended claim 3 as set forth above.

In response to the objection based on claims 40 and 41, the Office argues that the Figures do not show that the transistor structure has no gate insulator. Comparing Figure 1 (prior art) and Figure 2 depicts how the present application depicts that the transistor has no gate insulator.

Figure 1, representing the prior art, illustrates a transistor structure containing both a gate insulating layer (19) and a field oxide layer (17). Figure 2, representing the invention, only depicts a field oxide layer (170) and does not have a gate insulating layer (i.e., corresponding to the gate insulating layer 19 depicted in Figure 1). Thus, the Figures depict the absence of a gate insulating layer.

For these reasons, Applicant respectfully requests withdrawal of the objections to the Figures.

Rejection under 35 U.S.C. § 112, ¶ 1

The Office has rejected claims 40 and 41 under 35 U.S.C. § 112, ¶ 1 as containing non-enabled subject matter, e.g., the Office alleges that the present application shows a gate insulator but claims 40 and 41 recite a transistor without a gate insulator. Applicant respectfully traverses this rejection.

As discussed immediately above, Figure 2 depicts the transistor structure without a gate insulating layer. As well, the first line of paragraph 33 of the specification explicitly states, when discussing Figure 2, that "a thin gate insulating layer does not exist in the field transistor." While Figure 2 shows a field oxide layer (170), this is not the same as a gate insulating layer.

Thus, Applicant respectfully requests withdrawal of this rejection.

Rejection under 35 U.S.C. § 102 over Murakami et al.

The Office has rejected claims 1, 19, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Murakami et al. (U.S. Patent No. 5,623,154) for the reasons detailed on pages 3-7 of the Office Action. Applicant respectfully traverses this rejection.

The Office argues that Murakami et al. teach the claimed invention. In particular, the Office contends that Murakami et al. teach a field oxide layer (15) for defining an active region. Applicant respectfully disagrees with this interpretation of Murakami et al. This reference discloses an NMOS transistor 20 containing source and drain regions 11, a gate oxide film 15, and a gate electrode layer 17. The device of Murakami et al. also contains an isolating oxide film 5 which the skilled artisan would have understood to be a field oxide (FOX) layer based on how it is shown in Figure 1, how it is described, and how it is formed. *See column 1, lines 25-50 and Figure 1.* Thus, the Office is incorrect in arguing that Murakami et al. teach a field oxide layer 15. The part of the device of Murakami et al. labeled as 15 is a gate insulating layer, not a field oxide layer.

Further, the claims have been amended to include the limitation that the transistor structure contains no gate insulating layer. The Office has not shown that Murakami et al. teach the absence of a gate insulating layer. Indeed, it would be difficult for the Office to show that Murakami et al. teach the absence of a gate insulating layer since Figure 1 depicts a transistor structure with gate insulating layer 15.

Accordingly, the Office has not shown that Murakami et al. teach each and every limitation in these claims and Applicant respectfully requests withdrawal of this ground of rejection.

Rejection under 35 U.S.C. § 103 over Admitted Prior Art

The Office has rejected claims 1, 19, 27, and 29 under 35 U.S.C. § 103 as being unpatentable over Applicant's Admitted Prior Art (AAPA) for the reasons detailed on pages 7-13 of the Office Action. Applicant respectfully traverses this rejection.

The Office alleges that the AAPA (e.g., Figure 1) teaches the invention as claimed, including the high concentration source and drain regions adjacent low concentration source and drain regions. While the Office recognizes that Figure 1 itself does not teach this combination, the Office argues that the areas directly under the FOX layer 17 would be low concentration regions (LDD) and would have a lower dopant concentration than the remainder of source and drain regions because (1) the processing used to form source 14 and drain 15 would form a higher dopant concentration at the top of the layer than the bottom and (2) the FOX layer 17 would serve as a mask.

Applicants disagree with the Office's rationale which proffers no evidence, merely allegations. For example, it is not always the case that the dopant concentration of the upper part of a layer will be higher than the dopant concentration of the lower part of a layer because subsequent processing can be used to modify the dopant concentrations (e.g., "drive in" processes).

Nevertheless, in an effort to expedite prosecution, Applicant has amended the claims to include the limitation that the transistor structure contains no gate insulating layer. The Office has not shown that AAPA teach the absence of a gate insulating layer. Indeed, it would be difficult for the Office to show that AAPA suggests the absence of a gate insulating layer since Figure 1 depicts a transistor structure with gate insulating layer 19.

Accordingly, the Office has not shown that AAPA teaches or suggests every limitation in these claims and Applicant respectfully requests withdrawal of this ground of rejection.

Rejection under 35 U.S.C. § 103 over AAPA in view of Murakami et al.

The Office has rejected claims 2-10 and 20-28 under 35 U.S.C. § 103 as being unpatentable over AAPA in view of Murakami et al., for the reasons detailed on pages 13-22 of the Office Action. Applicant respectfully traverses this rejection.

As detailed above, the Office has not shown that AAPA (i.e., Figure 1) teaches or suggests the absence of a gate insulating layer in the transistor structure. And the Office has not shown that Murakami et al. teach the absence of a gate insulating layer. Indeed, it would be difficult for the Office to show that Murakami et al. suggest the absence of a gate insulating layer since Figure 1 depicts a transistor structure with gate insulating layer 15.

Thus, the Office has not shown that neither AAPA nor Murakami et al. alone teach or suggest the absence of a gate insulating layer in the transistor structure. And since neither reference alone teaches or suggests this limitation, it would extremely difficult for the Office to show that their combined disclosures would teach or suggest such a limitation.

Accordingly, the Office has not shown that the combination of AAPA and Murakami et al. teach or suggest every limitation in the present claims. Thus, Applicant respectfully requests withdrawal of this ground of rejection.

CONCLUSION

For the above reasons, as well as those of record, Applicant respectfully requests the Office to withdraw the pending grounds of rejection and allow the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 18-0013\40013.0001.

Respectfully Submitted,

By _____

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Date: January 21, 2003

APPENDIX A: MARKED-UP VERSION OF CLAIM AMENDMENTS

1. (Amended) A field transistor containing no gate insulating layer comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

3. (Amended) The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the [second] first conductivity type.

19. (Amended) A semiconductor device containing no gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over a portion of the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

27. (Amended) A semiconductor device containing no gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer;

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region;

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

29. (Amended) A system for electrostatic discharge protection containing a field transistor without a gate insulating layer, the field transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.